CHIP-INTERLEAVED BLOCK-SPREAD CDMA OR DS-CDMA FOR CELLULAR DOWNLINK?*

Geert Leus[1†], *Pengfei Xia*[2], *Shengli Zhou*[2], *Georgios B. Giannakis*[2]

[1] Katholieke Universiteit Leuven, Dept. of EE (ESAT), Kasteelpark Arenberg 10, 3001 Leuven, Belgium

[2] University of Minnesota, Dept. of ECE, 200 Union St. SE, Minneapolis, MN 55455, USA

ABSTRACT

Recently, a so-termed Chip-Interleaved Block-Spread (CIBS) CDMA system has been introduced, which enables Multi-User Interference (MUI) free reception. This transceiver can be used in the uplink as well as in the downlink. In this paper, we focus on the downlink and compare the downlink CIBS-CDMA system employing an MUI-free receiver with the conventional downlink Direct-Sequence (DS) CDMA system employing a chip equalizer receiver. The analysis, which is validated by simulation results, reveals that CIBS-CDMA with an MUI-free receiver has a number of advantages over DS-CDMA with a chip equalizer receiver.

1. INTRODUCTION

In a conventional downlink Direct-Sequence (DS) CDMA system, Multi-User Interference (MUI) can be removed completely in a frequency-flat fading channel, due to the spreading code orthogonality among different users. However, as the chip rate increases, the underlying channel becomes frequency-selective. Frequency-selectivity introduces Inter-Chip Interference (ICI), which destroys spreading code orthogonality at the receiver, and therefore causes MUI.

In [2], [1], [3], a class of chip equalizer receivers has been developed to suppress MUI in a downlink DS-CDMA system. This kind of receivers share the simple idea of first linearly equalizing the frequency-selective channel to restore completely, or partially, the multi-user signal transmitted from the base station at the chip rate, and then correlating the result with the spreading code to decode the information symbols of the desired user. DS-CDMA receivers equipped with Zero Forcing (ZF) or Minimum Mean Square Error (MMSE) chip equalizers have been shown to offer significant performance gains over the conventional RAKE receiver, [2], [1], [3].

Recently, a so-termed Chip-Interleaved Block-Spread (CIBS) CDMA system has been introduced, which maintains spreading code orthogonality at the receiver even after frequency-selective propagation, and thus enables MUI-free reception [5]. This transceiver can be used in the uplink as well as in the downlink. Focusing on the downlink, and comparing the downlink CIBS-CDMA system employing an MUI-free receiver with the downlink DS-CDMA system employing a chip equalizer receiver, we obtain the following interesting results:

- CIBS-CDMA systems with an MUI-free receiver guarantee channel-irrespective symbol recovery, whereas DS-CDMA systems with a chip equalizer receiver can only guarantee symbol detectability if one uses multi-antenna reception and/or oversampling, provided that the underlying channels have no common zeros.
- For a single-antenna reception that is not oversampled, CIBS-CDMA systems with an MUI-free receiver provide reliable bit error rate performance, whereas DS-CDMA systems with a chip equalizer receiver require multi-antenna reception and/or oversampling. However, since oversampling does not provide as much gain as multiple receive antennas, the use of multiple receive antennas is generally advocated, which increases the cost of the mobile.
- In CIBS-CDMA systems with an MUI-free receiver power control can be used effectively and optimal power allocation is simple, whereas in DS-CDMA systems with an MMSE chip equalizer receiver this is not the case.
- For the same spreading gain, the CIBS-CDMA system with an MUI-free receiver is generally less complex than the DS-CDMA system with a chip equalizer receiver.
- For the same spreading gain, both systems can afford approximately the same maximal intra-cell user load, and exhibit comparable robustness against inter-cell interference.
- For the same spreading gain, the CIBS-CDMA system with an MUI-free receiver outperforms the DS-CDMA system with a chip equalizer receiver, for moderate and high user loads.

Notation: Bold upper letters denote matrices, bold lower letters denote column vectors; $(\cdot)^T$, $(\cdot)^H$, and $(\cdot)^\dagger$ denote transpose, Hermitian transpose, and pseudo inverse respectively; $\otimes$ denotes the Kronecker product, and $\delta[\cdot]$ denotes the Kronecker delta; $\mathrm{E}\{\cdot\}$ stands for ensemble expectation; $\mathbf{I}_K$ denotes the $K \times K$ identity matrix, and $\mathbf{0}_{M\times N}$ denotes the $M \times N$ all zero matrix. In this paper, i is used for block index, k for symbol index, n for chip index, and u for user index.

2. UNIFYING SYSTEM MODEL

In this section, we present a unifying system model for downlink DS-CDMA and downlink CIBS-CDMA. At the base station, both systems convert the information symbol sequences $\{s_u[k]\}_{u=0}^{U-1}$, where $s_u[k]$ is the uth user's information symbol sequence, into a multi-user chip sequence $x[n]$. For both systems, this conversion can be viewed in a block spreading framework as follows: the information symbol sequence $s_u[k]$ is first serial-to-parallel converted into the sequence of $K \times 1$ information symbol blocks $\bar{\mathbf{s}}_u[i] := [s_u[iK], \ldots, s_u[(i+1)K-1]]^T$. Each $K \times 1$ information symbol block $\bar{\mathbf{s}}_u[i]$ is then spread by an $N \times M$ spreading matrix $\mathbf{C}_u[i]$ to obtain the $N \times 1$ chip block $\mathbf{x}_u[i] := \mathbf{C}_u[i]\bar{\mathbf{s}}_u[i]$. Each sequence of $N \times 1$ chip blocks $\mathbf{x}_u[i]$ is then weighted by a weight A_u to control the near-far effect, and the results are added

*This work was supported by NSF grants 9979443 and 0105612.

†Postdoctoral Fellow of the FWO-Vlaanderen (Belgium).

together to obtain the sequence of $N \times 1$ multi-user chip blocks

$$\mathbf{x}[i] := \sum_{u=0}^{U-1} A_u \mathbf{x}_u[i] = \sum_{u=0}^{U-1} A_u \mathbf{C}_u[i] \bar{\mathbf{s}}_u[i]. \quad (1)$$

The sequence of $N \times 1$ multi-user chip blocks $\mathbf{x}[i]$ is finally parallel-to-serial converted into the multi-user chip sequence $x[n]$, which in block form can be written as $[x[iN], \ldots, x[(i+1)N-1]]^T := \mathbf{x}[i]$. The difference between downlink DS-CDMA and downlink CIBS-CDMA then boils down to a difference in the design of $\mathbf{C}_u[i]$, which we will describe further on.

After the information symbol sequences $\{s_u[k]\}_{u=0}^{U-1}$ are converted into a multi-user chip sequence $x[n]$, the latter is transmitted at rate $1/T_c$. Suppose now that the desired mobile is equipped with M_r receive antennas, and that each receive antenna is sampled at rate M_s/T_c, where M_s denotes the oversampling factor. Then, the system can be viewed as having $M = M_r M_s$ outputs that are sampled at rate $1/T_c$. The received sequence at the mth output ($m \in \{0, 1, \ldots, M-1\}$) will be written as $y_m[n] = \sum_{l=0}^{L} h_m[l] x[n-l] + e_m[n]$, where $h_m[l]$ is the channel from the base station to the mth output with known upper bound on the order L, and $e_m[n]$ is additive noise at the mth output. If we serial-to-parallel convert the received sequence $y_m[n]$ into the sequence of $N \times 1$ received blocks $\mathbf{y}_m[i] := [y_m[iN], \ldots, y_m[(i+1)N-1]]^T$, and select the transmitted block size $N \geq L$, we obtain the following block model for the mth output:

$$\mathbf{y}_m[i] = \mathbf{H}_m^{(0)} \mathbf{x}[i] + \mathbf{H}_m^{(1)} \mathbf{x}[i-1] + \mathbf{e}_m[i], \quad (2)$$

where $\mathbf{H}_m^{(0)}$ is the lower triangular $N \times N$ Toeplitz matrix with first column $[h_m[0], \ldots, h_m[L], 0, \ldots, 0]^T$, $\mathbf{H}_m^{(1)}$ is the upper triangular $N \times N$ Toeplitz matrix with first row $[0, \ldots, 0, h_m[L], \ldots, h_m[1]]^T$, and $\mathbf{e}_m[i]$ is defined similar to $\mathbf{y}_m[i]$. The second term represents the so-called Inter-Block Interference (IBI).

Let us now describe the difference between downlink DS-CDMA and downlink CIBS-CDMA, which boils down to a difference in the design of $\mathbf{C}_u[i]$, as we mentioned before. Both systems assign to each user a distinct $P \times 1$ spreading code $\mathbf{c}_u$. Moreover, the spreading codes are designed to be mutually orthogonal, i.e., $\mathbf{c}_u^H \mathbf{c}_{u'} = \delta[u-u']$.

For *downlink DS-CDMA*, the spreading matrix $\mathbf{C}_u[i]$ is then designed as

$$\mathbf{C}_u[i] = \mathbf{T}\mathbf{D}_u[i], \text{ with } \mathbf{D}_u[i] = \mathbf{\Lambda}[i](\mathbf{I}_K \otimes \mathbf{c}_u), \quad (3)$$

where $\mathbf{T} := [\mathbf{I}_{KP}, \mathbf{0}_{KP \times L}]^T$, and $\mathbf{\Lambda}[i]$ is a $KP \times KP$ diagonal matrix holding on its diagonal the overlay (long scrambling) code symbols with modulus 1. Note that K should be viewed here as the frame length, which justifies the insertion of a zero guard through the matrix $\mathbf{T}$ in (3). At this point, let us also introduce the sequence of $KP \times 1$ chip blocks without zero-padding $\mathbf{z}_u[i] := \mathbf{D}_u[i] \bar{\mathbf{s}}_u[i]$, the corresponding sequence of $KP \times 1$ multi-user chip blocks

$$\mathbf{z}[i] := \sum_{u=0}^{U-1} A_u \mathbf{z}_u[i] = \sum_{u=0}^{U-1} A_u \mathbf{D}_u[i] \bar{\mathbf{s}}_u[i], \quad (4)$$

and the corresponding multi-user chip sequence $z[n]$, which in block form can be written as $[z[iKP], \ldots, z[(i+1)KP-1]]^T := \mathbf{z}[i]$.

For *downlink CIBS-CDMA*, on the other hand, the spreading matrix $\mathbf{C}_u[i]$ is then designed as

$$\mathbf{C}_u[i] = \mathbf{D}_u[i] \bar{\mathbf{T}}, \text{ with } \mathbf{D}_u[i] = (\bar{\mathbf{\Lambda}}[i] \mathbf{c}_u) \otimes \mathbf{I}_{K+L}, \quad (5)$$

where $\bar{\mathbf{T}} := [\mathbf{I}_K, \mathbf{0}_{K \times L}]^T$, and $\bar{\mathbf{\Lambda}}[i]$ is a $K \times K$ diagonal matrix holding on its diagonal the overlay (long scrambling) code symbols with modulus 1.

Observing from (1) and (2) that both designs remove the IBI, since $\mathbf{H}_m^{(1)} \mathbf{C}_u[i-1] = \mathbf{0}_{N \times K}$, $\forall u \in \{0, 1, \ldots, U-1\}$, both systems can be described in a unified form by the following IBI-free model for the mth output:

$$\begin{aligned} \mathbf{y}_m[i] &= \mathbf{H}_m^{(0)} \mathbf{x}[i] + \mathbf{e}_m[i] \\ &= \mathbf{H}_m^{(0)} \left(\sum_{u=0}^{U-1} A_u \mathbf{C}_u[i] \bar{\mathbf{s}}_u[i] \right) + \mathbf{e}_m[i]. \end{aligned} \quad (6)$$

Stacking $\{\mathbf{y}_m[i]\}_{m=0}^{M-1}$ as $\mathbf{y}[i] := [\mathbf{y}_0^T[i], \ldots, \mathbf{y}_{M-1}^T[i]]^T$, we can thus write

$$\begin{aligned} \mathbf{y}[i] &= \mathbf{H}^{(0)} \mathbf{x}[i] + \mathbf{e}[i] \\ &= \mathbf{H}^{(0)} \left(\sum_{u=0}^{U-1} A_u \mathbf{C}_u[i] \bar{\mathbf{s}}_u[i] \right) + \mathbf{e}[i], \end{aligned} \quad (7)$$

where $\mathbf{H}^{(0)} := [\mathbf{H}_0^{(0)T}, \ldots, \mathbf{H}_{M-1}^{(0)T}]^T$, and $\mathbf{e}[i]$ is defined similar to $\mathbf{y}[i]$. Using this unifying system model, we next describe the chip equalizer receiver for downlink DS-CDMA, and the MUI-free receiver for downlink CIBS-CDMA.

2.1. Chip Equalizer Receiver for Downlink DS-CDMA

Using (1), (3), and (4), we obtain that $\mathbf{x}[i] = \mathbf{T}\mathbf{z}[i]$. Hence, we can rewrite (7) as

$$\mathbf{y}[i] = \mathbf{H}^{(0)} \mathbf{x}[i] + \mathbf{e}[i] = \mathbf{H}^{(0)} \mathbf{T} \mathbf{z}[i] + \mathbf{e}[i].$$

The chip equalizer receiver now equalizes $\mathbf{y}[i]$ in order to obtain an estimate for $\mathbf{z}[i]$, using a block chip equalizer $\mathbf{G} = [\mathbf{G}_0, \ldots, \mathbf{G}_{M-1}]$, where $\mathbf{G}_m$ is a $KP \times (KP+L)$ Toeplitz matrix with first column $[g_m[D], \ldots, g_m[L_g], 0, \ldots, 0]^T$, and first row $[g_m[D], \ldots, g_m[0], 0, \ldots, 0]$, with $g_m[l]$ denoting the L_gth order chip equalizer for the mth antenna. Note that this formulation introduces a delay of D chips. As an estimate for $\mathbf{z}[i]$, we then obtain

$$\begin{aligned} \hat{\mathbf{z}}[i] &= \mathbf{G}\mathbf{y}[i] = \mathbf{G}\mathbf{H}^{(0)} \mathbf{T} \mathbf{z}[i] + \mathbf{G}\mathbf{e}[i] \\ &= \mathbf{Y}[i]\mathbf{g} = \mathbf{Z}[i]\boldsymbol{\mathcal{H}}\mathbf{g} + \mathbf{E}[i]\mathbf{g}, \end{aligned} \quad (8)$$

where $\mathbf{Y}[i] := [\mathbf{Y}_0[i], \ldots, \mathbf{Y}_{M-1}[i]]$, with $\mathbf{Y}_m[i]$ a $KP \times (L_g+1)$ Toeplitz matrix with first column $[y_m[i(KP+L)+D], \ldots, y_m[i(KP+L)+D+KP-1]]^T$ and first row $[y_m[i(KP+L)+D], \ldots, y_m[i(KP+L)], 0, \ldots, 0]$, $\mathbf{g} := [\mathbf{g}_0^T, \ldots, \mathbf{g}_{M-1}^T]^T$, with $\mathbf{g}_m := [g_m[0], \ldots, g_m[L_g]]^T$, $\mathbf{Z}[i]$ is a $KP \times (L+L_g+1)$ Toeplitz matrix with first column $[z[iKP+D], \ldots, z[(i+1)KP-1], 0, \ldots, 0]^T$ and first row $[z[iKP+D], \ldots, z[iKP], 0, \ldots, 0]$, $\boldsymbol{\mathcal{H}} := [\boldsymbol{\mathcal{H}}_0, \ldots, \boldsymbol{\mathcal{H}}_{M-1}]$, with $\boldsymbol{\mathcal{H}}_m$ the $(L+L_g+1) \times (L_g+1)$ Toeplitz matrix with first column $[h_m[0], \ldots, h_m[L], 0, \ldots, 0]^T$ and first row $[h_m[0], 0, \ldots, 0]$, and $\mathbf{E}[i]$ is defined similar to $\mathbf{Y}[i]$. The third equality in (8) is basically due to the commutativity of the convolution operator.

Note that the Zero-Forcing (ZF) chip equalizer $\mathbf{g}$ only exists if the $(L+L_g+1) \times M(L_g+1)$ channel matrix $\boldsymbol{\mathcal{H}}$ has full row rank $L+L_g+1$, which requires $M(L_g+1) \geq L+L_g+1$, and the channels $\{h_m[l]\}_{m=0}^{M-1}$ to have no common zeros. Let us now assume that the sequence $z[n]$ is white with variance σ_z^2, the sequences $\{e_m[n]\}_{m=0}^{M-1}$ are mutually uncorrelated and white with

variance σ_e^2, and $K \to \infty$. The ZF and MMSE chip equalizers can then be expressed respectively as:

$$\mathbf{g}^{ZF} = \boldsymbol{\mathcal{H}}^H(\boldsymbol{\mathcal{H}}\boldsymbol{\mathcal{H}}^H)^{-1}\mathbf{i}_D,$$
$$\mathbf{g}^{MMSE} = \boldsymbol{\mathcal{H}}^H(\boldsymbol{\mathcal{H}}\boldsymbol{\mathcal{H}}^H + (\sigma_e^2/\sigma_z^2)\mathbf{I}_{L+L_g+1})^{-1}\mathbf{i}_D,$$

where $\mathbf{i}_D$ denotes the $(L+L_g+1)\times 1$ unit vector with a one in the $(D+1)$st position. These expressions correspond to the ones presented in [3], and will be used to perform the simulations.

Exploiting the fact that $\mathbf{D}_u[i]$ possesses mutual orthogonality among users, the chip equalizer receiver then despreads $\hat{\mathbf{z}}[i]$ with $(1/A_u)\mathbf{D}_u[i]$ in order to obtain an estimate for $\bar{\mathbf{s}}_u[i]$:

$$\hat{\bar{\mathbf{s}}}_u[i] = (1/A_u)\mathbf{D}_u^H[i]\hat{\mathbf{z}}[i]. \tag{9}$$

2.2. MUI-free Receiver for Downlink CIBS-CDMA

Using (5), we obtain from [5] that $\mathbf{C}_u[i]$ lies in the column space of $\mathbf{D}_u[i]$ after propagation through a frequency-selective channel: $\mathbf{H}_m^{(0)}\mathbf{C}_u[i] = \mathbf{D}_u[i]\bar{\mathbf{H}}_m^{(0)}\bar{\mathbf{T}}$, where $\bar{\mathbf{H}}_m^{(0)}$ is the $(K+L)\times(K+L)$ lower triangular Toeplitz matrix with first column $[h_m[0],\ldots,h_m[L],0,\ldots,0]^T$. Hence, we can rewrite (6) as

$$\begin{aligned}\mathbf{y}_m[i] &= \mathbf{H}_m^{(0)}\left(\sum_{u=0}^{U-1} A_u\mathbf{C}_u[i]\bar{\mathbf{s}}_u[i]\right) + \mathbf{e}_m[i] \\ &= \sum_{u=0}^{U-1} A_u\mathbf{D}_u[i]\bar{\mathbf{H}}_m^{(0)}\bar{\mathbf{T}}\bar{\mathbf{s}}_u[i] + \mathbf{e}_m[i].\end{aligned} \tag{10}$$

Exploiting the fact that $\mathbf{D}_u[i]$ possesses mutual orthogonality among users, the MUI-free receiver now despreads $\mathbf{y}_m[i]$ with $(1/A_u)\mathbf{D}_u[i]$ in order to obtain an MUI-free output for the mth output of the uth user:

$$\bar{\mathbf{y}}_{u,m}[i] = (1/A_u)\mathbf{D}_u^H[i]\mathbf{y}_m[i] = \bar{\mathbf{H}}_m^{(0)}\bar{\mathbf{T}}\bar{\mathbf{s}}_u[i] + \bar{\mathbf{e}}_{u,m}[i],$$

where $\bar{\mathbf{e}}_{u,m}[i]$ is defined similar to $\bar{\mathbf{y}}_{u,m}[i]$. Stacking $\{\bar{\mathbf{y}}_{u,m}[i]\}_{m=0}^{M-1}$ as $\bar{\mathbf{y}}_u[i] := [\bar{\mathbf{y}}_{u,0}^T[i],\ldots,\bar{\mathbf{y}}_{u,M-1}^T[i]]^T$, we can thus write

$$\bar{\mathbf{y}}_u[i] = \bar{\mathbf{H}}^{(0)}\bar{\mathbf{T}}\bar{\mathbf{s}}_u[i] + \bar{\mathbf{e}}_u[i], \tag{11}$$

where $\bar{\mathbf{H}}^{(0)} := [\bar{\mathbf{H}}_0^{(0)T},\ldots,\bar{\mathbf{H}}_{M-1}^{(0)T}]^T$, and $\bar{\mathbf{e}}_u[i]$ is defined similar to $\bar{\mathbf{y}}_u[i]$.

The MUI-free receiver then equalizes $\bar{\mathbf{y}}_u[i]$ in order to obtain an estimate for $\bar{\mathbf{s}}_u[i]$, using a block symbol equalizer $\bar{\mathbf{G}}_u := [\bar{\mathbf{G}}_{u,0},\ldots,\bar{\mathbf{G}}_{u,M-1}]$, where $\bar{\mathbf{G}}_{u,m}$ is a $K\times(K+L)$ matrix with no particular structure. As an estimate for $\bar{\mathbf{s}}_u[i]$, we then obtain:

$$\hat{\bar{\mathbf{s}}}_u[i] = \bar{\mathbf{G}}_u\bar{\mathbf{y}}_u[i] = \bar{\mathbf{G}}_u\bar{\mathbf{H}}^{(0)}\bar{\mathbf{T}}\bar{\mathbf{s}}_u[i] + \bar{\mathbf{G}}_u\bar{\mathbf{e}}_u[i]. \tag{12}$$

Note that the ZF block symbol equalizer $\bar{\mathbf{G}}_u$ always exists, since the $(K+L)\times K$ channel matrix $\bar{\mathbf{H}}_m^{(0)}\bar{\mathbf{T}}$ by construction has full column rank K, regardless of the channel $h_m[l]$; and thus, the $M(K+L)\times K$ channel matrix $\bar{\mathbf{H}}^{(0)}\bar{\mathbf{T}}$ also has full column rank K, regardless of the channels $\{h_m[l]\}_{m=0}^{M-1}$. Let us now assume that the sequence $s_u[k]$ is white with variance σ_s^2, and the sequences $\{e_m[n]\}_{m=0}^{M-1}$ are mutually uncorrelated and white with variance σ_e^2. The ZF and MMSE block symbol equalizers can then be expressed respectively as:

$$\bar{\mathbf{G}}_u^{ZF} = (\bar{\mathbf{H}}^H\bar{\mathbf{H}})^{-1}\bar{\mathbf{H}}^H,$$
$$\bar{\mathbf{G}}_u^{MMSE} = (\bar{\mathbf{H}}^H\bar{\mathbf{H}} + \sigma_e^2/(A_u^2\sigma_s^2)\mathbf{I}_K)^{-1}\bar{\mathbf{H}}^H.$$

These expressions will be used to perform the simulations.

3. CIBS-CDMA VS. DS-CDMA COMPARISONS

3.1. Symbol Detectability

In CIBS-CDMA systems employing an MUI-free receiver, channel-irrespective symbol detectability is guaranteed, since the $M(K+L)\times K$ channel matrix $\bar{\mathbf{H}}^{(0)}\bar{\mathbf{T}}$ in (11) has full column rank K, regardless of the channels $\{h_m[l]\}_{m=0}^{M-1}$. For DS-CDMA systems employing a chip equalizer receiver, on the other hand, symbol detectability can only be guaranteed if the $(L+L_g+1)\times M(L_g+1)$ channel matrix $\boldsymbol{\mathcal{H}}$ in (8) has full row rank $L+L_g+1$, i.e., if $M(L_g+1)\geq L+L_g+1$, which requires $M>1$, and the channels $\{h_m[l]\}_{m=0}^{M-1}$ have no common zeros. Hence, channel-irrespective symbol detectability can never be guaranteed. From the equivalence between symbol detectability and diversity gain [4], we deduce that the CIBS-CDMA system enjoys a larger diversity gain than the DS-CDMA system.

3.2. Single Antenna vs. Multiple Antennas

For $M=1$, CIBS-CDMA systems with an MUI-free receiver provide a reliable bit error rate performance. For DS-CDMA systems, on the other hand, it is clear from the previous paragraph that for $M=1$ the ZF chip equalizer receiver does not exist, and the performance of the MMSE receiver saturates at high SNR. Hence, we need $M>1$. However, since oversampling does not bring as much gain as multiple receive antennas, previous papers strongly propose to use multiple receive antennas, which of course increases the cost of the mobile.

3.3. Power Control

It is well-known that power control should be used in the downlink to combat near-far effects. Specifically, since faraway users see more power attenuation than nearby users, we may want to transmit more power towards the faraway users than towards the nearby users. However, if the users are not completely decoupled, the nearby users will see more interference due to the power boost for faraway users, and the overall system performance will drop. This is the case for downlink DS-CDMA systems with an MMSE chip equalizer receiver. Hence, in such systems, power control can not be used effectively, and optimal power allocation is complicated. Downlink CIBS-CDMA systems with an MUI-free receiver, on the other hand, completely decouple the users. Hence, increasing the transmit power of a certain user will not affect the performance of the other users. Therefore, power control can be used effectively, and optimal power allocation is simple.

3.4. Complexity

To make more detailed comparisons between both systems, let us from now on assume a constant spreading gain G. Hence, we assume

$$G = \frac{K_{ds}P_{ds}+L}{K_{ds}} = \frac{(K_{cibs}+L)P_{cibs}}{K_{cibs}}, \tag{13}$$

where K_{ds} and K_{cibs} denote the information block size for DS-CDMA and CIBS-CDMA, respectively, and P_{ds} and P_{cibs} denote the code length for DS-CDMA and CIBS-CDMA, respectively. Since the chip equalizer receiver is designed to be applied on larger blocks than the MUI-free receiver, we further assume

$$K_{ds} > K_{cibs}. \tag{14}$$

The complexity of the chip equalizer receiver and the MUI-free receiver can be expressed as $M(L_g + 1)P_{ds} + P_{ds}$ and $M(K_{cibs} + L) + M(K_{cibs} + L)/K_{cibs}P_{cibs}$ multiply-add operations per symbol, respectively. For both expressions, the first term corresponds to the equalization complexity, and the second term to the despreading complexity. Generally, the MUI-free receiver is less complex than the chip equalizer receiver. To illustrate this, choose $K_{cibs} \gg L$. From (13) and (14), we then obtain $G \approx P_{ds} \approx P_{cibs}$. In this case, the MUI-free receiver is less complex than the chip equalizer receiver if $K_{cibs} < L_g G + G/M$, which is generally the case, even though K_{cibs} is chosen to satisfy: $K_{cibs} \gg L$.

3.5. Maximal Intra-cell User Load and Inter-Cell Interference

The maximal intra-cell user load as well as the robustness against inter-cell interference (using the overlay code) are closely related, since they both depend on P. From (13) and (14), it is clear that $P_{ds} > P_{cibs}$, which would mean that the DS-CDMA system can afford a higher maximal intra-cell user load, and is more robust against inter-cell interference than the CIBS-CDMA system. However, when choosing $K_{cibs} \gg L$, we obtain $G \approx P_{ds} \approx P_{cibs}$, as discussed above, and both systems can afford approximately the same maximal intra-cell user load, and exhibit comparable robustness against inter-cell interference. In this context, note also that the performance of the MUI-free receiver does not depend on the intra-cell user load U, while the performance of the MMSE chip equalizer decreases with increasing U. This is also illustrated in the next section.

3.6. Simulations

Let us now take a look at some performance results, assuming there is no inter-cell interference, and the different users have equal power. We consider a chip rate of $1/T_c = 1.2288$ MHz. Focusing on a delay spread of about 10 μs, we assume 4 equal power Rayleigh fading paths with the first positioned 12 chips away from the last, and the other two positioned randomly in between. We further consider a root raised cosine filter at transmitter and receiver, with roll-off factor $\alpha = 0.22$, and truncated after 5 chips on each side. Hence, as an upper bound on the channel order we may take $L = 32$. We further consider BPSK signaling, and take $K_{ds} = 508$, $K_{cibs} = 127$, $P_{ds} = 40$, $P_{cibs} = 32$, and $L_g = L = 32$. Note that for this set of parameters, both (13) and (14) are satisfied, and the MUI-free receiver is less complex than the chip equalizer receiver. To keep the simulation time small, we have chosen the difference between P_{ds} and P_{cibs} not too small, but in practice this difference can be taken much smaller in order to guarantee approximately the same maximal intra-cell user load, and comparable robustness against inter-cell interference (see previous subsection). Figure 1 shows analytical and simulation results for both systems. Clearly, the ZF chip equalizer performs much worse than the MMSE chip equalizer. The bad performance of the ZF chip equalizer is due to the excessive noise enhancement this equalizer causes in the presence of ill-conditioned channels. The ZF and MMSE block symbol equalizers applied in the MUI-free receiver, on the other hand, have similar performance. Furthermore, for the same number of receive antennas M_r, oversampling factor M_s, and user load U, the CIBS-CDMA system with an MUI-free receiver outperforms the DS-CDMA system with a chip equalizer receiver, if the user load U is not too small.

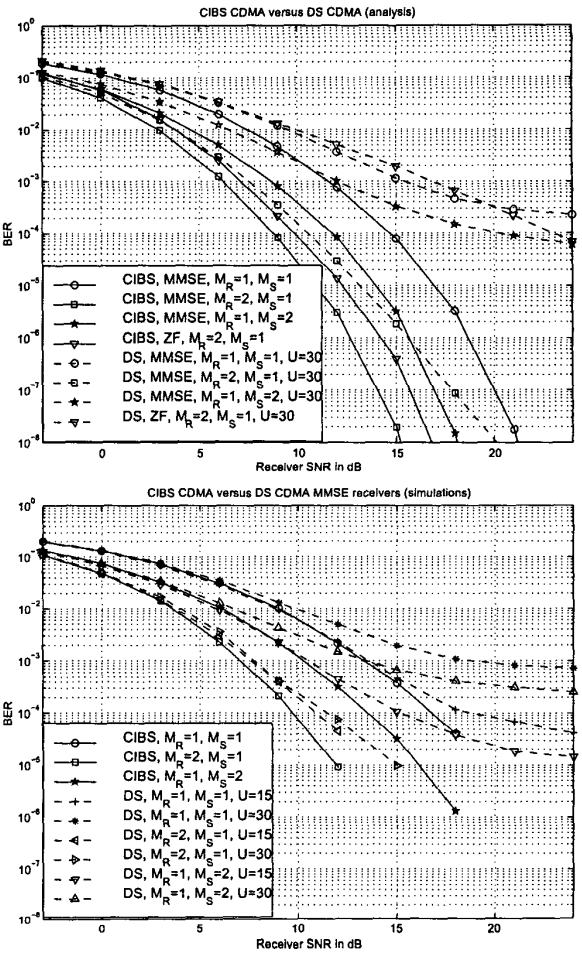

Fig. 1. Performance comparison: DS-CDMA vs. CIBS-CDMA.

4. REFERENCES

[1] I. Ghauri and D. T. M. Slock, "Linear receivers for the DS-CDMA downlink exploiting orthogonality of spreading sequences," in *Proc. of Asilomar Conf. on Signals, Systems, and Computers*, November 1998, vol. 1, pp. 650–654.

[2] A. Klein, "Data detection algorithms specially designed for the downlink of CDMA mobile radio systems," in *Proc. of Vehicular Techn. Conf.*, May 1997, vol. 1, pp. 203–207.

[3] T. P. Krauss, W. J. Hillery, and M. D. Zolotowski, "Downlink specific linear equalization for frequency selective CDMA cellular systems," *Journal of VLSI Signal Processing*, 2001.

[4] Z. Wang and G. B. Giannakis, "Linearly Precoded or Coded OFDM against Wireless Channel Fades?," in *Proc. of IEEE Workshop on Signal Processing Adv. in Wireless Commun.*, Taoyuan, Taiwan, R.O.C., pp. 267–270, April 2001.

[5] S. Zhou, G. B. Giannakis, and C. Le Martret, "Chip interleaved block spread code division multiple access," *IEEE Transaction on Communications*, 2002 (to appear).